IN THE CLAIMS

Please amend claims 14, 16, 17, 20 and add newly submitted claims 26 and 27 as indicated below:

1. (Previously Cancelled)

2. (Previously Cancelled)

3. (Previously Cancelled)

4. (Previously Cancelled)

5. (Previously Cancelled)

6. (Previously Cancelled)

7. (Previously Cancelled)

8. (Previously Cancelled)

9. (Previously Cancelled)

10. (Previously Cancelled)

11. (Previously Cancelled)

12. (Previously Cancelled)

13. (Previously Cancelled)

14. (Currently Amended) An apparatus for testing the electrical characteristics of a semiconductor integrated circuit, said apparatus comprising:

an outer layer surrounding an inside needle, which can be drawn back and then released for subsequent probing and testing operations by said inside needle; and

said outer layer comprising a hard dielectric material, which can penetrate through a semiconductor layer to permit subsequent testing of at least one semiconductor integrated circuit component located below said semiconductor layer.

15. (Unamended) The apparatus of claim 14 wherein said inside needle is adapted to electrically contact said at least one semiconductor integrated circuit component located below said semiconductor layer.

16. (Currently Amended) The apparatus of claim 14 wherein said inside needle comprises a metal prober.

17. (Currently Amended) The apparatus of claim 14 wherein said outer layer comprises a piercer in a shape of hard dielectric sheath.

18. (Unamended) The apparatus of claim 14 wherein said outer layer comprises diamond.

19. (Previously Cancelled)

20. (Currently Amended) The apparatus of claim 16 ~~14~~ wherein said ~~inside needle comprises a conductive~~ metal prober comprises a conductive metal.

21. (Unamended) The apparatus of claim 14 wherein said inside needle and said outer layer together form a concentric double layer structure prober.

22. (Unamended) The apparatus of claim 14 wherein said outer layer comprises a sheath formed from a hard dielectric material, such that said sheath comprises a piercer.

23. (Previously Cancelled)
24. (Previously Cancelled)
25. (Previously Cancelled)
26. (Previously Cancelled)

27. (Newly Submitted) A combined piercer/prober apparatus for testing the electrical characteristics of a semiconductor integrated circuit, said apparatus comprising:

a piercer in a shape of a hard dielectric sheath comprising an outer layer;

a prober formed from an inner layer in a shape of an inside needle surrounded by said outer layer, wherein said prober can be drawn back while said piercer penetrates at least one semiconductor integrated circuit located below said semiconductor layer for subsequent probing and testing thereof by said prober and wherein said inside needle is adapted to electrically contact said at least one semiconductor integrated circuit component located below said semiconductor layer; and

wherein said piercer and said prober together comprise a combined piercer/prober pen-shaped apparatus for testing the electrical characteristics of said at least one semiconductor integrated circuit.

28. (Newly Submitted) A combined piercer/prober apparatus for testing the electrical characteristics of a semiconductor integrated circuit, said apparatus comprising:

a piercer in a shape of a hard dielectric sheath comprising an outer layer surrounding an inner layer in a shape of an inside needle;

a prober formed from and comprising said inner layer wherein said prober can be drawn back while said piercer penetrates at least one semiconductor integrated circuit located below said semiconductor layer for subsequent probing and testing thereof by said prober;

wherein said inside needle and said outer layer together form a concentric double layer structure prober and wherein said inside needle is adapted to electrically contact said at least one semiconductor integrated circuit component located below said semiconductor layer; and

wherein said piercer and said prober together comprise a combined piercer/prober pen-shaped apparatus for testing the electrical characteristics of said at least semiconductor integrated circuit.